#13/Dec. 10/29/02

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 8, 2002

In re the application of:

James R. Del Signore II et al.

Filed: January 29, 2001

Ser. No. 09/770,478

For: Current Inrush Limiting Circuit

Docket No. 230 P 051

Art Unit: 2816

Examiner: Quan Tra

Confirmation No. 6823

DECLARATION UNDER 37 CFR 1.131

I, Randolph Bullock, declare as follows:

1. I have a BS degree in Electrical Engineering from Rochester Institute of Technology, awarded 1979.

2. I have worked as an Electrical Engineer at Axiohm Transaction Solutions, Inc. ("Axiohm"), the Assignee of the present application, for the past 4 years, and am a co-inventor on the present invention.

3. It is required practice of the engineers at Axiohm that we maintain dated laboratory notebooks to chronologically document our work.

4. I first conceived of the invention that is described and claimed in the present application prior to September 15, 1999. For instance, I have laboratory notebook entries dated prior to September 15, 1999 (dates redacted for confidentiality reasons), that show the circuit that is the subject of the present application, and is essentially reproduced as Figure 2 in the present

application. A copy of this laboratory notebook page (with date redacted) is annexed hereto as Exhibit A.

5. I diligently reduced the circuit that is shown in Exhibit A into actual practice by building and testing breadboard models of the circuit, the first of which was built and tested in 1999. For instance, annexed hereto as Exhibit B is a memo I wrote (with date redacted) regarding some problems and corrective actions taken on the circuit that is the subject of the present invention during a design review process.

6. Throughout the year 2000, Axiohm engineers and technicians tested the circuit and continued to improve its performance. It is common that it takes at least a year worth of product testing and evaluation from the time of conception until an actual reduction to practice to complete the quality control necessary to release a new circuit, such as the one that is the subject of the present application, into the market. From the date of conception of the present circuit until the time of filing the present application and the subsequent actual reduction of practice of the circuit, I along with other Axiohm engineers and technicians diligently worked on development of the circuit that is the subject of the present application.

7. We filed the present patent application on January 29, 2001, and continued to diligently actually reduce the circuit to practice. Annexed hereto as Exhibit C is a memo I prepared subsequent to the filing of the present application (date redacted), revealing the results of further testing that was conducted on the present circuit.

All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application and any registration resulting therefrom.

Dated: 6-26-02

Randolph Bullock

Your mailroom stamp hereon acknowledge your safe receipt of:
the 2 page amendment and declaration with exhibits a - c

James R. Del Signore II et al.
Filed: January 29, 2001
Ser. No. 09/770,478
Art Unit: 2816
Confirmation No. 6823
For: Current Inrush Limiting Circuit

Our Docket No. 230 P 051

July 23, 2002
GRM/arm

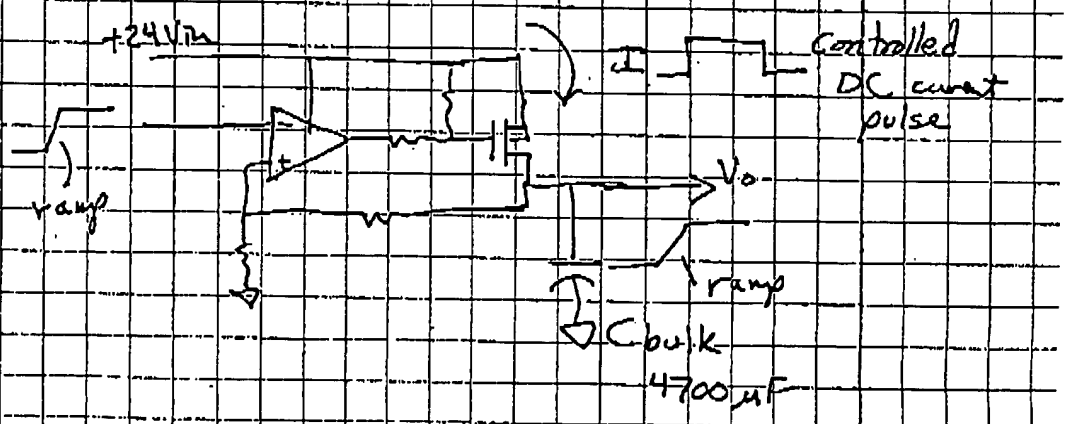
USB - A758 xlab

1. Review R13/R14
2. Check LED status
3. Notes re: flush parts
4. Q16/R11 height + lay flat
5. 6.00 MHz Resonator?

→ Better inrush control: — next USB board spin

Apply controlled voltage ramp to bulk capacitor —
Voltage ramp ⇒ Constant current into C.

- Linear op amp w/ feedback from voltage output
- No current sense shunt.
- Set at < normal peak printing current
- Test w/ NCR term + bricked SNI Beetle.



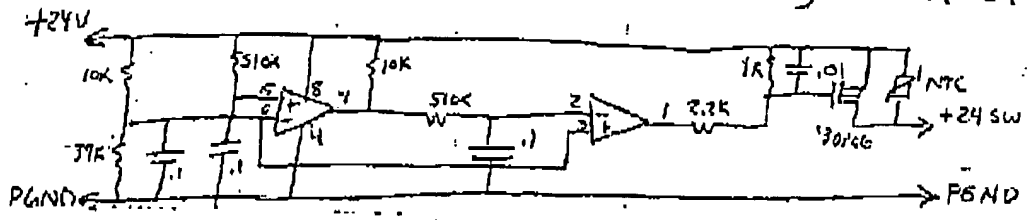
A794/A758 Inrush Control Review

Thoughts:

1. Does A794 need inrush control at all; with only 100µF bulk capacitance I doubt it.
   ⇒ Remove inrush circuit from all A794 option boards if inrush is below limit (Measure max. inrush into 1000µF)

2. Current inrush ckt. works fine as long as 1st charge cycle is very close to full before FET turns on; ckt. has many parts, could be simpler.
   Concern: a) Secondary current pulse can be large depending on lots of variables...
   b) Total charge-up time [illegible]

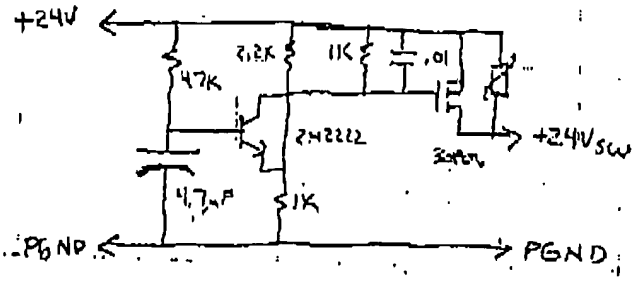
3. Keep present ckt. but remove the NPN, switch U1 pins 2+3



$I_{pk} = 3A$ $I_{rms} = 2A$ (50ms) $T_{delay} = 350ms$

This works fine, exactly as previous circuit but less 1 SOT-23 NPN and 1 resistor

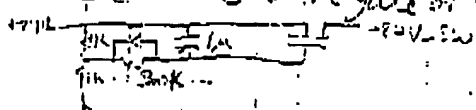
4. Do we need a dual comparator for this delay function? No.



With this circuit, a softer turn-on of the FET allows shorter delay.

$I_{pk} = 3A$ $I_{rms} = 2A$ (50ms) $T_{delay} = 200ms$

5. ND77 (SMI) uses an R-C at the gate of the P-Fet

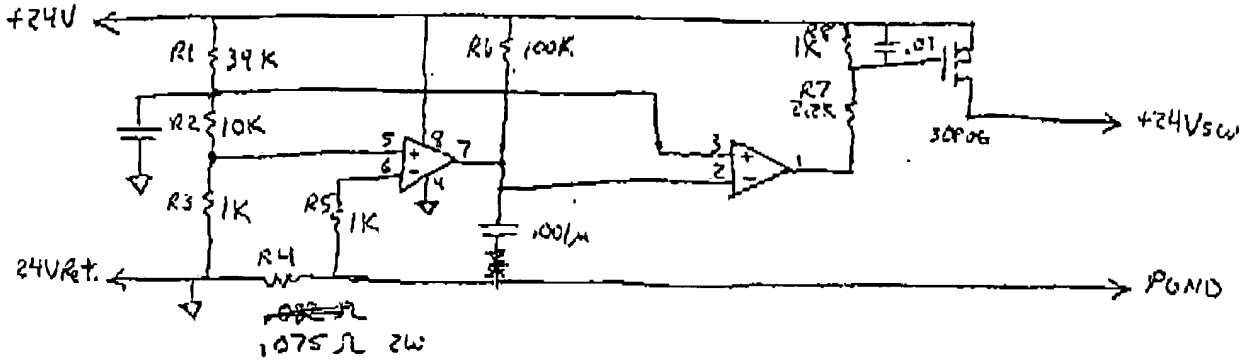


A799/A758 Inrush Control Review (continued from p. 34)

5. B Alternate approach – get rid of NTC thermistor, keep comparator, but re-configure as a chopper current-limiting device.

a) Whenever current draw exceeds setpoint, FET is turned off for a short time before re-enabled. This would be set well above the DC supply rating so that normal print operation doesn't trigger the circuit. During startup (1st supply connection or power-on) and fault conditions the switcher would kick in.

b) During normal oper., FET is ON continuously.



I_{pk} = 7A I_{rms} = 3A T_{delay} = 60 ms

Recommend change .075Ω to .082 Ω

⇒ I_p = 6.4A I_{rms} = 2.7A T_{delay} = 66 ms

Max DC drop in R4 = 0.53 V

c) If concern re. early chop during print, raise set-point as long as terminal supply can handle higher I_{pk}.

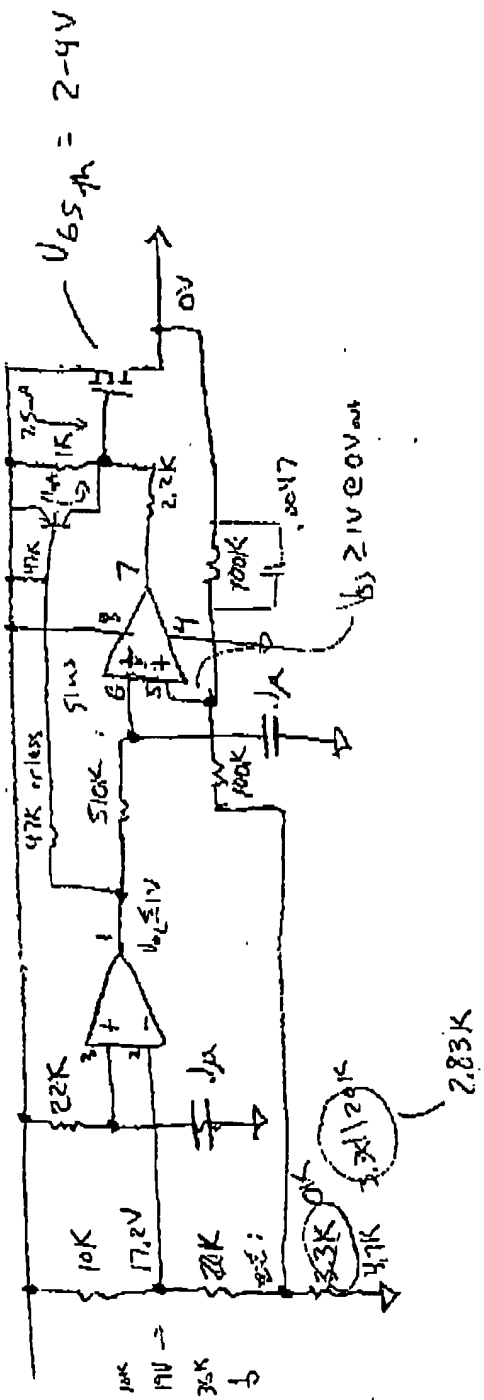
Switch freq. = 50 kHz
Current rise/fall time = 1.7A/μs max ⇒ no harmonics past 50KHz. (as measured)

A758 Inrush Analysis/Test

w/o control Inrush = 65Apk X .1ms
+ 30Apk X 3ms
+ 5A X 30ms

w/chop control, Inrush = 6Apk X 200ms. (0.1Ω)
→ but it resets during Print!
w/chop control @ .05Ω, Inrush = 11Apk X 7.5ms.
→ No Reset
we have 7A peaks during 42 col. 50% duty bars
(6.7A measured) spaced 4ms apart

[redacted]



Prototype voltage-ramp inrush control circuit for M257, M282 USB boards.

Developed Fall, 99. RB 6-25-02

Axiohm
Making Global Impressions™

From: Randy Bullock
To: Scott Lewis
Cc: Mike Franzen, Denny Coon, Jim DelSignore, Bob McCarney, Barry Shaw, Mike Gera, Rick George, Bob Delaney
Date:
Subject: Design Review for A758/A794 USB/RS232 Serial Option PCBA, artwork number M257/M282.

Attendees: Scott Lewis, Barb Clise, George Kellogg, Barry Shaw, Jim DelSignore, Larry Jensen, Randy Bullock

A design review was held to assess the readiness of board design M257 and M282 for prototype builds at BSU, with production release to follow qualification testing. These designs implement the USB interface, along with an RS232 (9-pin) interface, on A758 and A794 option boards, respectively. The following describes the changes made, with reference to current (M245) parts locations:

	Problem:	Action:
1.	A-model had moderate emissions peak over Class-B lim at 90-100MHz	Added 330 Ohm bus termination resistors on all address, data, and control lines, added ferrites to lines leaving the board.
2.	Retention of RS232 interface beyond prototype phase required making it consistent with current production RS232 design.	Return to use of the HIN-208 interface IC, return of ferrites o I/O lines, re-hookup of RTS and CTS lines borrowed for possible diagnostic uses on A-model, move 9-pin connector u to the plate for proper ground termination, not hidden inside.
3.	LED was located poorly for interface to the sheet metal.	Move LED to a more-carefully designed location where a peep-hole can be located in the metal shield.
4.	Time allowed the development and prototyping of a new lower-cost inrush circuit having no PTC thermistor.	Added new circuit, but retained locations where the original circuit may be populated in the interim.
5.	Review logic supply connections with regard to future 3.3V system.	Move source pins to pins designated +Vd,Dgnd on the printer bus interface. Otherwise, the A-model design was already 3.3V ready, by a jumper.

During the design review, the following questions were raised:

	Question:	Action:
1.	Should we have a pullup on U3 pin 8 instead of hard-wire?	Better from design and testability, so pullup was added.
2.	Have resistors been checked for dissipation ratings?	Yes, since A794 board (M282) uses 0603 size and arrays, som had to be checked. Where needed, larger sizes were retained, such as for LED ballast.
3.	Has 5V/3.3V compatibility been addressed?	Yes, with reference to the latest A794 parallel (1284) design.
4.	Do we really want to change a working inrush circuit?	Although this new circuit will save about $0.80 per board, it can be put off until further testing has been done. Both new and old circuits can be used in the current artwork.
5.	Is the USB signal path EXACTLY per the book?	Yes, except for two added ferrites. Decided to change them such that they could be individually changed back to resistors, not stuck inside an array with other functions. Trace routings are carefully balanced and direct.
6.	Do we need to terminate unused Address lines (A1,2)?	While it may theoretically be a good idea, if none of the other option boards have worried about unused lines, this must not b an issue for Class-B compliance of these printers.
7.	We should remove all inner-plane copper from the areas between isolation ferrites and the Com connectors.	Done for both USB and RS232 connectors.

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To: Jim Del Signore Date:

Cc: Kyle Turner, Terry Wildey

Subject: Recent abnormal behavior of 55W power supplies used in conjunction with USB interface boards in A758 printers.

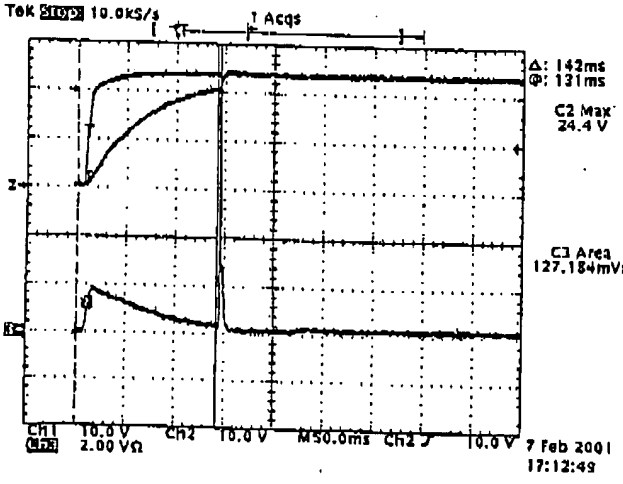
Statement of Problem:
A758 USB/RS232 (F354) printers in Extended Test (Wed. Feb. 7th) have been found to "trip" a standard 55W brick power supply when plugged in from an already-warmed-up state (of both brick and printer). Once the combination tripped, it would continue to cycle with the brick coming up, going into current-limit shutdown, then retrying after a timeout.

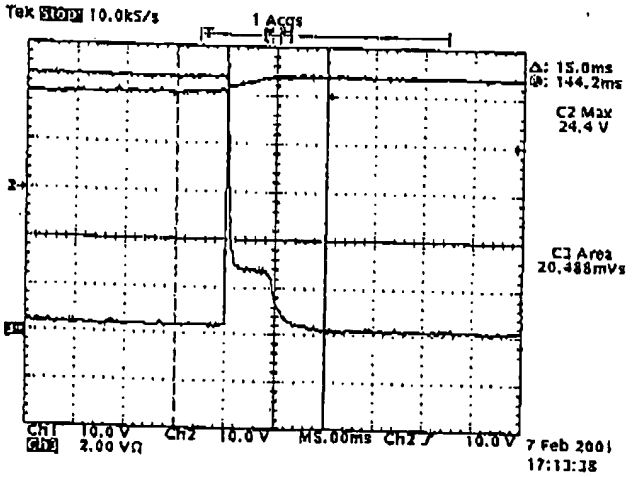
Background:
Prior to Acceptance Tests, the NCR powered configuration was extensively tested over temperature extremes while applying worse-than-spec loads to the circuit. The brick systems were tested during Acceptance using a small sample of printers and power supplies, at nominal circuit values, and over normal operating environment ranges, but failed to uncover this shortfall. The Lead Year supply was known to be capable of bringing up uncontrolled 4700uF bulk capacitors in 7156, while the NCR terminal was known to trip in that situation. Since inrush situations are by nature transient, out-of-DC-spec events, there was no indication that a pulse exceeding DC rating by only 50%, lasting for 32ms, could trip the "more rugged" 55W supply, while presenting no challenge whatever to the "sensitive" NCR terminal supply.

Root cause appears to be that the level at which the current is fed to the 4700uF capacitor inside the A758 is above the 2.3A rating of the 55W brick for the 32ms duration of the charging pulse. Note that the peak current under the USB inrush circuit is well below that of the Serial board with thermistor. The circuit was developed primarily to allow hot-plugging of NCR terminal (7452, 7453) supplies to printers.

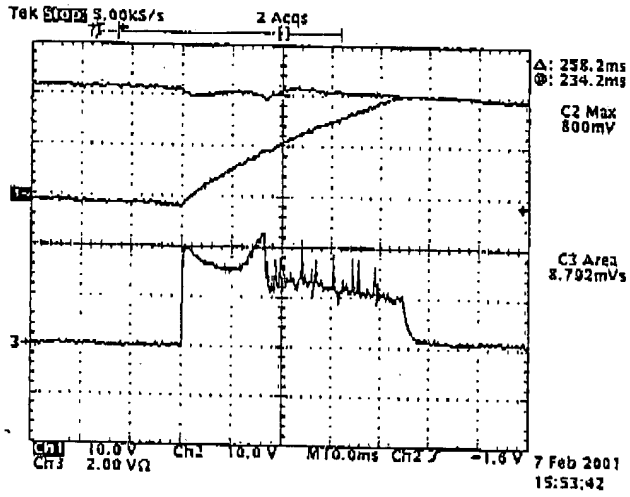
Below are scope traces of the typical inrush current and voltage waveforms seen in both A758 and A794 printers. In all shots, top traces are input and output voltage from the inrush circuit, bottom trace is input current drawn from the supply, 2V/div=2A/div.

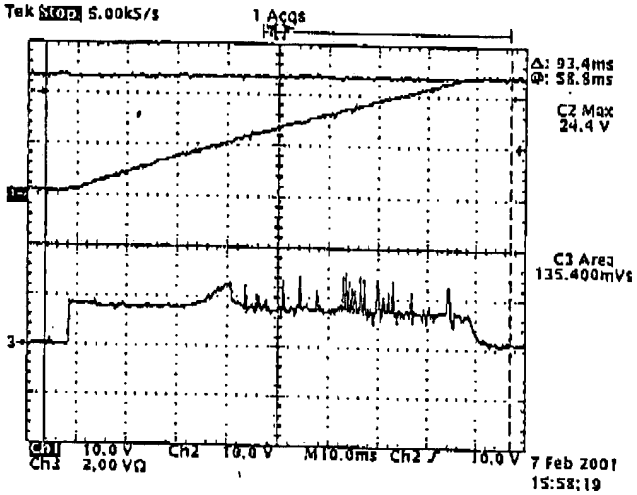
First, A758 with RS232 option. At right is an expanded view of the second pulse.

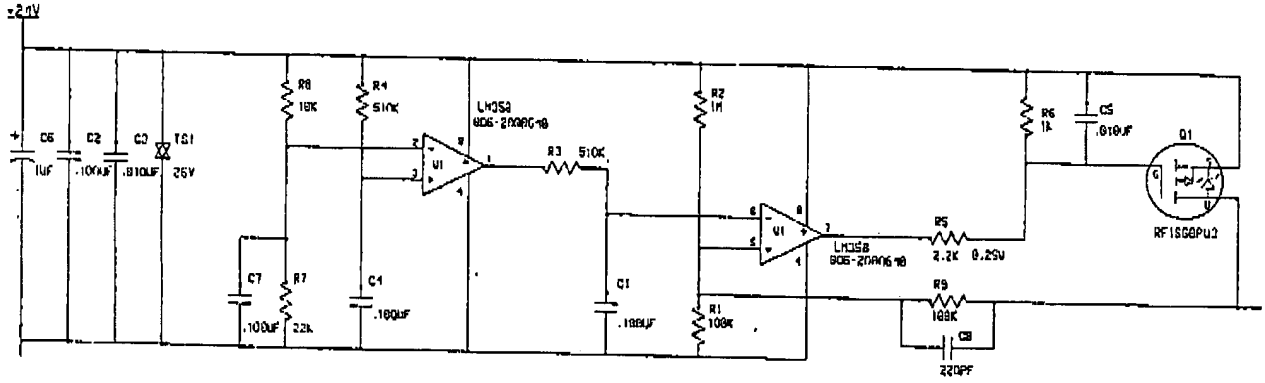




Next, we see the USB option with inrush pulse. At left is today's circuit which is quite acceptable on NCR 7452 and 7453 series terminal power supplies but has been found to fold-back some previously warmed-up Lead Year 55W bricks. At right is the proposed solution, in which R3 is increased from 510K to 1Meg, thereby doubling the time it takes to charge the bulk capacitor and halving the current required, from 3.5A to under 2A. This is then well within the rating of both the 55W brick, and any potential customer's 48W terminal supplies.

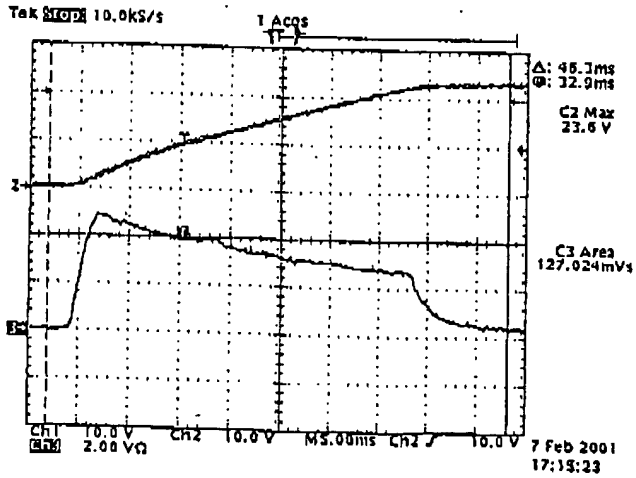


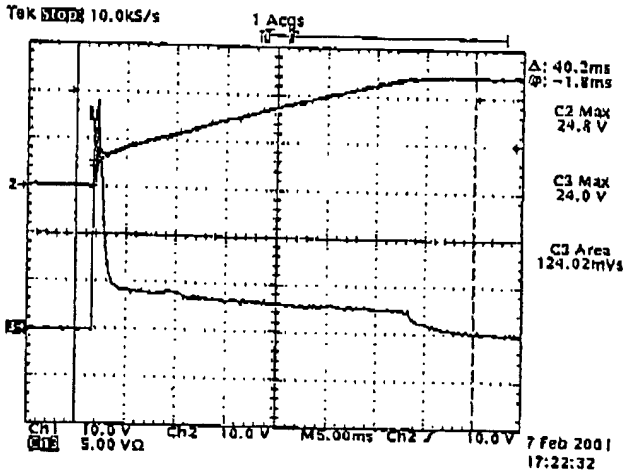




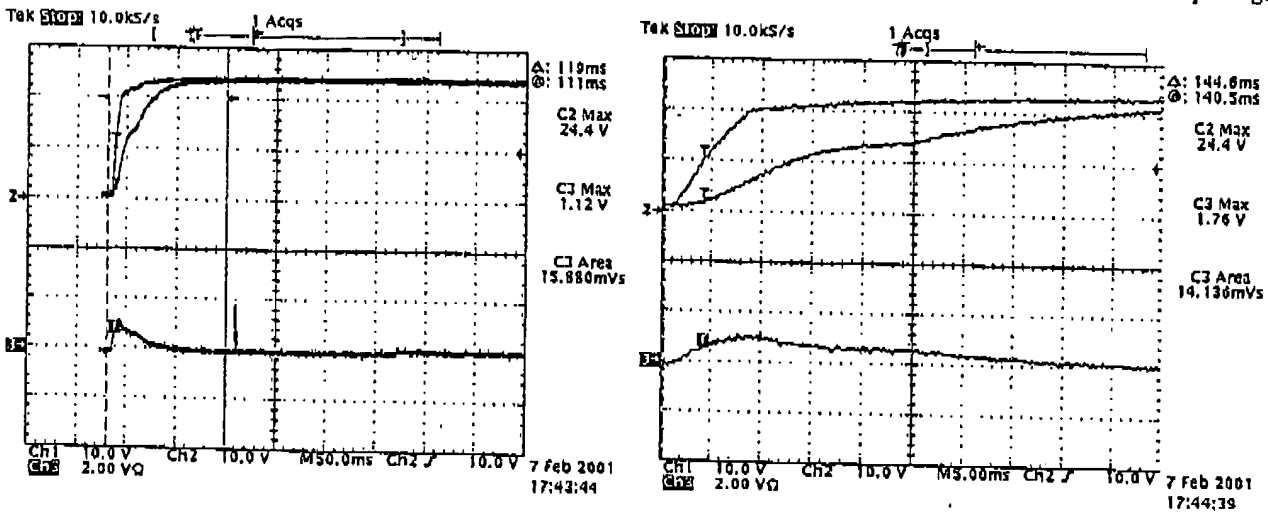
Present A758 USB inrush control circuit.

Below are shots of an uncontrolled inrush into A758, at left when the AC side of the brick is connected, at right when the DC side is hot-connected, bypassing the inrush circuit. Note the current scale at right is 5A/div, not 2A, as in all other shots. Unlimited inrush reaches 24A when the DC side is hot-connected, but only 5A when the supply is allowed to bring up the printer on application of its AC supply.

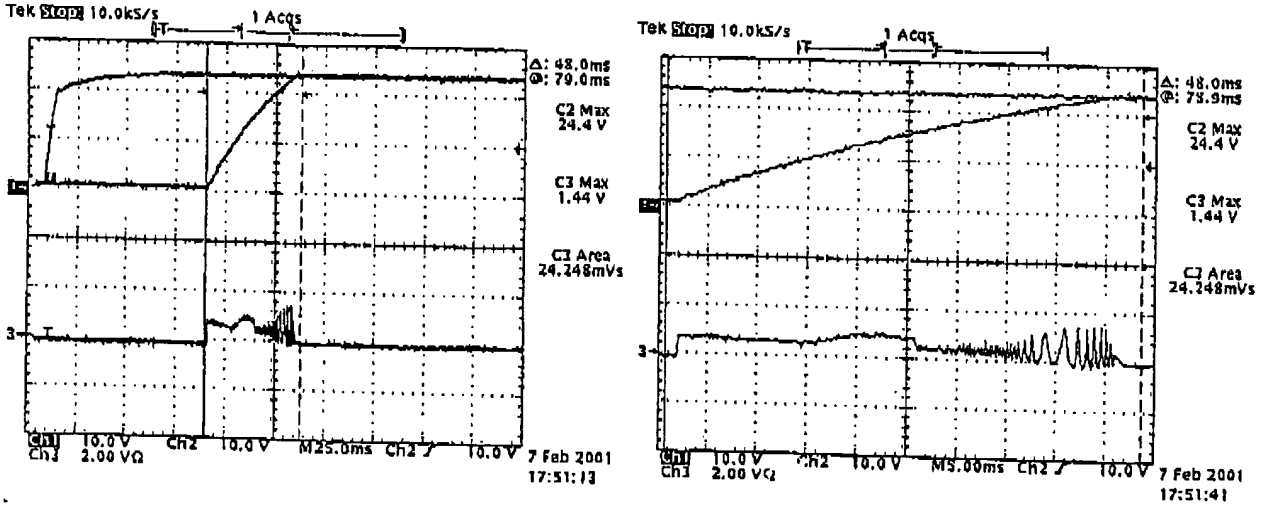




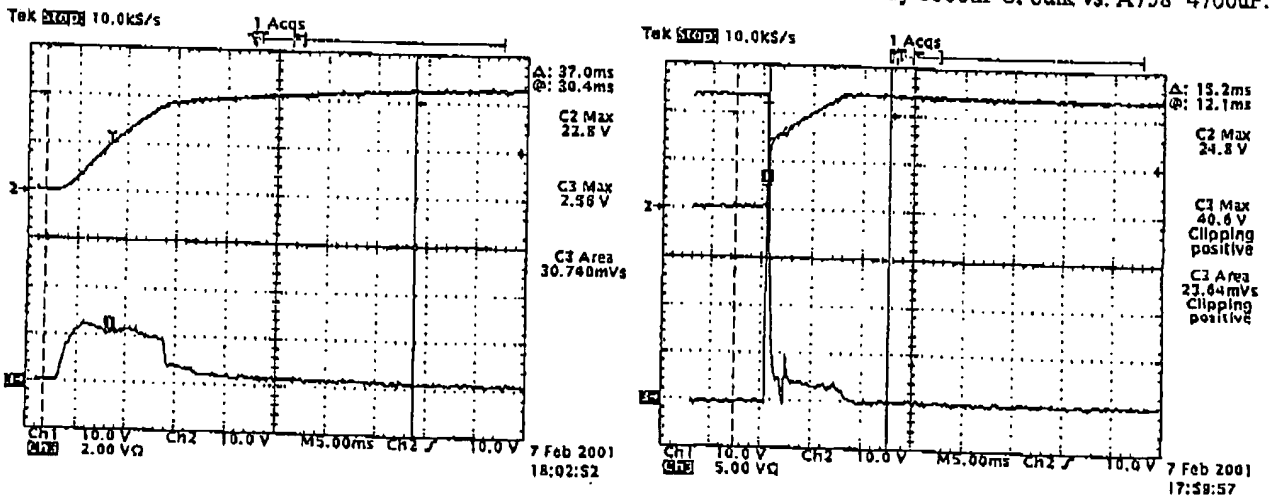
A very relevant question is "What about A794?" Here is inrush current to A794, through RS232 option, with close-up at right.



Here is A794 inrush current connected to USB/RS232 option, with close-up at right.



Finally, the A794 without inrush limiting, when AC connected or DC connected. Although the peak current is higher than A758 due to low ESR of the smaller bulk capacitor, total energy is much less, as A794 has only 1000uF of bulk vs. A758' 4700uF.



Appendix A - A758 Inrush Limiter Test Plan

Introduction

In order to prove the suitability of a new lower-cost inrush limiting circuit design, tests must verify that the circuit operates as intended over operating ambient conditions, and with outside-limit parts tolerances. Since the specific requirement that drove the development of this feature was a limitation of the NCR terminal power supplies, the NCR 7452 terminal will be used as the power source and test criteria for this test.

Test Cases

1. Functional test. This is intended to verify that in all respects, at 25°C, the new circuit design is at least equal to the existing.
2. Operating Environmental – temperature. The same sequence used in test (1) will be repeated at the limits of temperature.
3. Operating Environmental – voltage. Since it is not feasible to modify the terminal's output voltage, bench tests over the operating supply range should be done to demonstrate the circuit operation over supply voltage variations.
4. EMC tests. These will show that there is no adverse reaction to expected ESD events, nor degradation of present emissions characteristics.

Test Procedures

Functional Test: (PE Lab)

Use an A758 (any vintage), add an additional 4700uF capacitor across the 24V system inside the printer, with a 125 Ohm, 10W resistor across that for a bleeder. Install a modified (Rev. C) USB B-model (M257) option board. For power, use a 7452 power cord with the +24V lead brought out and cut, to connect power to the printer from the terminal. A pulse generator will operate a switching device in series with the power cord to connect and disconnect the +24V lead to the printer power jack (1 sec ON, 4 sec OFF) for the duration of the test (5760 cycles per 8hr shift).

Pass Criteria: The terminal remains powered-up throughout the test. Failure is noted by the terminal and printer turning off upon closure of the power switch to the printer. The terminal cannot automatically recover from this event, so it will be a hard failure requiring unplugging and reconnecting of the AC line cord to the terminal.

Status: Complete, no failure through 8 hours at room temperature.

Operating Environmental Temperature Test: (PE Lab)

Same setup as Functional, except run over 5-50°C temperature in the chamber, 8 hours at 5C, 8 hours at 50C.

Pass Criteria: Same as Functional.

Status: Complete, no failure through both 8 hour runs at 5C and 50C temperatures.

Operating Environmental Voltage Test: (PE Lab)

Same setup as Functional, except supply from a variable bench supply over 21.6-26.4V. Record current waveform using current probe on +24V lead, with scope Measurements – RMS, Peak functions applied to the first 100ms of the trace following closure of the switch.

Pass Criteria: Instantaneous peak current not to exceed 20A, nor any peaks greater than 10A for more than 10ms.

Status: Complete, peak currents less than specified limits and duration.

EMC Tests – ESD Immunity, Emissions: (Eng Lab)

One modified USB option board (Rev. C) unit sent to Curtis-Straus installed in "99 production" style controller, shall be subjected to standard Class B emissions and ESD testing up to 6KV contact, 12KV air discharge.

Pass Criteria: The modified inrush circuit shall remain fully-ON (no power interruption or false restart) during ESD testing. It shall not adversely impact the emissions characteristics of the production A758.

Status: Complete, no adverse impact on EMC, per Eng lab tests and Curtis-Straus WO#A0422 test report.

2:53 PM 10/28/02 Transmission Record
Received from remote ID "3154713167"
Unique ID: "QTR3DBD4F734E9A"
Elapsed time: 6 minutes, 16 seconds.
Used channel 4.
No ANI data.
No AOC data.
Resulting status code (0): No Errors
Pages sent: 1 - 17

Counselors At Law
HANCOCK Estabrook, LLP

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TO: Quan Tra	FAX #: 703-746-7234
RE: U.S. Patent Appln. Ser. No. 09/770,478 in the name of James R. Del Signore II, et al; Title: Current Inrush Limiting Circuit; Our Docket No. 230 P 051	
FROM: Sue Denny	DATE/TIME: October 28, 2002
CLIENT ACCT.: 104960	CLIENT MATTER #: 38

NUMBER OF PAGES TELECOPIED 17 (INCLUDING COVER PAGE)

REMARKS: **Dear Mr. Tra: In accordance with your instructions during our telephone conversation of this afternoon, following (16pp) is a copy of the attorney of record's response to your final Official Action which was dated May 31, 2002.**

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